

## CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

forming a dielectric spacer layer overlying a gate structure formed on a semiconductor substrate; and

etching said dielectric spacer layer without the use of a sacrificial forming spacer to form L-shaped spacers for the gate structure, the L-shaped spacers including a horizontal portion having a thickness that varies gradually to provide for an average thickness of the horizontal portion that is 50 to 85 percent of a maximum thickness of the horizontal portion, wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L-shaped spacers, said L-shaped spacers have vertical portions varying in thickness and horizontal portions varying in thickness, the horizontal portions have bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portions to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer.

2. - 18. (Canceled)

19. (Currently Amended) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

forming a dielectric spacer layer over the semiconductor substrate having a first exposed surface portion adjacent to a first sidewall of a gate structure and a second exposed surface portion adjacent to a second sidewall of the gate structure; and etching said first and second exposed surface portions of the dielectric spacer layer while forming first and second L-shaped spacers for the gate structure at respective locations of the first and second exposed surface portions, wherein etching forms

an L-shaped spacer having a vertical portion varying in thickness and a horizontal portion varying in thickness, the horizontal portion varying in thickness to provide an average thickness that is 50 to 85 percent of a maximum thickness of the horizontal portion, wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form said L-shaped spacers, said horizontal portions of the L-shaped spacers have bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portions of the L-shaped spacers to a portion of the L-shaped spacers furthest from the vertical portion of the L-shaped spacer.

20. (Previously Presented) The method of Claim 19, further including forming a liner oxide layer over said gate structure prior to forming the dielectric spacer layer.

21. (Previously Presented) The method of Claim 20 wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.

22. (Previously Presented) The method of Claim 19 wherein said dielectric spacer layer comprises a nitride layer.

23. (Previously Presented) The method of Claim 21, wherein the said dielectric spacer layer has a thickness in the range of 150 Angstroms and 500 Angstroms.

24. (Previously Presented) The method of Claim 19 wherein said dielectric spacer layer comprises a silicon oxynitride layer.

25. (Canceled)

26. (Canceled)

27. (Currently Amended) The method of Claim ~~[[25]]1~~, wherein said dielectric spacer layer is anisotropically etched using a capacitively coupled plasma etch process with an etching

chemistry comprising CH<sub>3</sub>F and O<sub>2</sub> in combination with an inert gas to form said L-shaped spacers.

28. (Currently Amended) The method of Claim [[25]]1, wherein said dielectric spacer layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH<sub>3</sub>F and O<sub>2</sub> in combination with an inert gas.

29. (Previously Presented) The method of Claim 19, wherein etching said dielectric spacer layer to form said L-shaped spacers includes using CH<sub>3</sub>F and O<sub>2</sub> chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH<sub>3</sub>F to O<sub>2</sub>.

30. (Previously Presented) The method of Claim 29, wherein etching said dielectric spacer layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.

31. (Previously Presented) The method of Claim 29, wherein etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.

32. (Canceled)

33. (Canceled)

34. (Previously Presented) The method of Claim 1, further including forming a liner oxide layer over said gate structure prior to forming the dielectric spacer layer.

35. (Previously Presented) The method of Claim 34, wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.

36. (Previously Presented) The method of Claim 1, wherein said dielectric spacer layer comprises a nitride layer.

37. (Previously Presented) The method of Claim 35, wherein the said dielectric spacer has a thickness in the range of 150 Angstroms and 500 Angstroms.

38. (Previously Presented) The method of Claim 1, wherein said dielectric spacer layer comprises a silicon oxynitride layer.

39. (Canceled)

40. (Canceled)

41. (Currently Amended) The method of Claim ~~[[39]]~~1, wherein said dielectric spacer layer is anisotropically etched using a capacitively coupled plasma etch process with an etching chemistry comprising CH<sub>3</sub>F and O<sub>2</sub> in combination with an inert gas to form said L-shaped spacers.

42. (Currently Amended) The method of Claim ~~[[39]]~~1, wherein said dielectric spacer layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH<sub>3</sub>F and O<sub>2</sub> in combination with an inert gas.

43. (Previously Presented) The method of Claim 1, wherein etching said dielectric spacer layer to form said L-shaped spacers includes using CH<sub>3</sub>F and O<sub>2</sub> chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH<sub>3</sub>F to O<sub>2</sub>.

44. (Previously Presented) The method of Claim 43, wherein etching said dielectric spacer layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.

45. (Previously Presented) The method of Claim 43, wherein etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.